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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,884	10/23/2006	Carl J. Knudsen	US03 0014 US	6212

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EXAMINER	
ABRISHAMKAR, KAVEH	
ART UNIT	**PAPER NUMBER**
2431	

NOTIFICATION DATE	DELIVERY MODE
11/04/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/541,884	KNUDSEN, CARL J.	
	Examiner	Art Unit	
	KAVEH ABRISHAMKAR	2431	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12, 15, 18, and 20-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-12,15,18 and 20-30* is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This amendment is in response to the amendment filed on June 30, 2009. Claims 1-25 were previously pending consideration. Per the received amendment, claims 13, 14, 16, 17, 19 are cancelled, and claims 26-30 are added.

2. Claims 1-12, 15, 18, and 20-30 are currently pending consideration.

Response to Arguments

3. Claims 10-12, 15, 18, and 20-30 are allowed.

4. Applicant's arguments filed June 30, 2009 with respect to claims 1-9 have been fully considered but they are not persuasive for the following reasons:

5. Regarding claim 1, the Applicant argues that the Cited Prior Art (CPA), Kommerling, does not disclose a sense circuit comprising a register configured to store selected bits of the plurality of magnetically-responsive nodes. This argument is not found persuasive. The CPA discloses that each sensor (sense circuit) is allocated a one-bit value (selected bit) (column 9, lines 46-48). Therefore, it is asserted that the CPA does disclose a sense circuit which comprises a register which stores selected bits of the plurality of magnetically-responsive nodes. Therefore, the rejection is maintained as given below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Kommerling et al. (US 7,005,733).

Regarding Claim 1:

Kommerling discloses an integrated circuit chip (“Integrated Circuit of Microchip,” See fig. 1b ref. no. 195 and col. 6 lines 24-30) with circuitry therein including a plurality of magnetically-responsive nodes adapted to store bits ("Hall Effect Sensors” See figs. 1a, 1b, 5a, and 5b ref. no. 150 and “Another is to allocate to each sensor a one bit value indicating whether it’s reading exceeds a threshold (derived initially based on the statistics of the readings) or not.” See col. 9 lines 46-48), a package having magnetic material covering at least a portion of circuitry in the integrated circuit chip (“The encapsulation 50 surrounds the device substrate 350 on both sides and comprises an epoxy resin matrix. Within the matrix, a plurality of particles 360 are provided, of various sizes, shapes and/or magnetic permeabilities." See col. 10 lines 44-52), and a sense circuit comprising a register configured to store selected bits of the plurality of magnetically-responsive nodes (“Sense Amplifier” See fig. 3 ref. no. 300 and col. 9 lines

20-32 [The examiner respectfully points out that the sense amplifier stores the bits read from the hall effect sensor while amplifying the voltages to a full logic high or a logic low.]), the bits defining a value as a function of the magnetic material in the package ("Thus, magnetic properties measured by the sensors 150 will generally be different at each of the sensors, as described above." See col. 11 lines 1-3), wherein the package and the plurality of magnetically-responsive nodes being arranged such that altering the package results in a state change of at least one of the plurality of magnetically-responsive nodes, the state change being detectable by the sense circuit ("Further, any attempt to remove the outer shield 370 will itself change the distribution of the magnetic field and therefore make it impossible to read the key." See col. 11 lines 4-6).

Regarding Claim 2:

Kommerling discloses the integrated circuit chip arrangement includes an enable register adapted to store selected bits of the plurality of magnetically-responsive nodes, the value of the bits being responsive to the magnetic material in the package ("The successive digital sensor readings are then loaded into a linear feedback shift register (LFSR) 330," See fig. 3 ref. no. 330 and col. 9 lines 33-37).

Regarding Claim 3:

Kommerling discloses a cryptographic key is formed from the bits having data stored in the enable register ("The successive digital sensor readings are then loaded into a linear feedback shift register (LFSR) 330 which combines them according to some scrambling function and produces a key 340 of the required length (e.g. 64 bits)

using all sensor readings, in some logical combination." See fig. 3 ref. no. 340 and col. 9 lines 33-37).

Regarding Claim 4:

Kommerling discloses the integrated chip arrangement is adapted for encrypting data as a function of the cryptographic key generated using the bits having data stored in the enable register ("The encryption/decryption unit 120 operates to encrypt and decrypt using an encryption key 160 provided from a cryptographic input unit 130." See col. 5 lines 52-59).

Regarding Claim 5:

Kommerling discloses a power-up state machine coupled to the enable register and coupled to the sense circuit ("Acquisition Logic" See figs. 1b and 3 ref. no. 197 and col. 6 lines 31-57).

Regarding Claim 6:

Kommerling discloses the selected magnetically stored bits are read to decrypt encrypted data ("The encryption/decryption unit 120 operates to encrypt and decrypt using an encryption key 160 provided from a cryptographic input unit 130." See col. 5 lines 52-59).

Regarding Claims 7-8:

Kommerling discloses the integrated circuit chip is further adapted to mask an output read from the magnetically-responsive nodes using the data stored in the enable register ("The successive digital sensor readings are then loaded into a linear feedback shift register (LFSR) 330 which combines them according to some scrambling function

and produces a key 340 of the required length (e.g. 64 bits) using all sensor readings, in some logical combination." See fig. 3 ref. no. 340 and col. 9 lines 33-37 [The examiner respectfully points out that the LFSR is hardwired to perform the scrambling function.]) and to store the masked output in an output register (The examiner respectfully points out that the key is stored in a register in the encryption/decryption unit. See fig. 1 ref. no. 120, col. 5 lines 60-67, col. 6 lines 1-16, and col. 7 lines 18-21), the contents of the output register being used for encrypting data ("The encryption/decryption unit 120 operates to encrypt and decrypt using an encryption key 160 provided from a cryptographic input unit 130." See col. 5 lines 52-59).

Regarding Claim 9:

Kommerling discloses the output register is configured and arranged to erase data stored therein upon power loss ("When power is removed, in step 1108 the registers in the encryption/decryption unit 120 and cryptographic input unit 130 are flushed to erase the key." See col. 7 lines 18-21), and wherein the enable register is adapted to mask an output read from the magnetically-responsive nodes stored in the output register upon restoring power to the output register ("On powering up, the circuit is arranged to read the detected property data 140 in step 1102 and to form a key as before in step 1104 (corresponding to step 1002 and 1004 discussed above.)" See col. 7 lines 13-21).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAVEH ABRISHAMKAR whose telephone number is (571)272-3786. The examiner can normally be reached on Monday thru Friday 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Korzuch can be reached on 571-272-7589. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kaveh Abrishamkar/
Primary Examiner, Art Unit 2431

/K. A./
10/30/2009
Primary Examiner, Art Unit 2431